S/N 08/903,453

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.
Examiner: George C. Eckert II
Serial No.: 08/903,453
Group Art Unit: 2815
Filed: July 29, 1997
Docket: 303.378US1
Title: CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS

#34 Response FJONES 4-12-02

RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

In response to the Office Action dated 21 December 2001, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 2, 3, 24-28, 41-48, 50-52, and 65-68 are pending in the application, and are rejected. None of the claims have been amended.

Telephone interview

The applicant thanks Examiner Eckert for the telephone interview granted on Thursday 14 March 2002, between himself and the applicant's representative Mr. Mates (Reg. No. 35,271). The substance of the following remarks were discussed in the interview.

Double Patenting Rejection

Claims 2 and 3 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims in co-pending Application No. 08/902,843. The applicant will address this rejection when the claims are otherwise indicated as allowable.

Rejection of Claims under §103

Claims 2, 3, 24-28, 41-48, 50-52, and 65-68 were rejected under 35 USC § 103(a) as being unpatentable over Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata), in view of Sugita et al. (JP Patent No. 08-255878, Sugita) and Burns et al., *Principles of Electronic Circuits* , pp. 382-383 (Burns). The applicant respectfully traverses.

Claim 24 recites a transistor comprising a source region in a substrate, a drain region in the substrate, a channel region between the source region and the drain region in the substrate, and a gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

Sakata shows in Figure 1 a heterojunction (HJ) diode structure comprising c-Si, a layer of hydrogenated amorphous silicon carbide (a-SiC:H), a layer of hydrogenated amorphous silicon (a-Si:H), another layer of a-SiC:H, and Al. Sakata, Column 3. Sakata is deficient as a reference in that Sakata does not show a source region in a substrate, a drain region in the substrate, and a channel region between the source region and the drain region in the substrate as are recited in claim 24.

Sugita shows a floating gate transistor with a source and a drain in a substrate, and a polysilicon floating gate separated from the substrate by an insulator.

However, there is no suggestion or motivation to combine Sakata and Sugita.

"To establish a *prima facie* case of obviousness ... there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP 2143.

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." MPEP 2143.01.

There are substantial differences in the priciples of operation of the HJ diode structure of Sakata and the floating gate transistor of Sugita. The HJ diode structure of Sakata is also referred to as "stacked insulator layers" through which both electrons and holes conduct. The principles of operation of the HJ diode structure of Sakata is described as follows:

> "With the application of positive (negative) bias to the metal gate, electrons (holes) are efficiently injected from the crystalline Si (c-Si) substrate into the thin a-Si:H layer through the compositionally graded a-SiC:H layer. When the bias voltage is restored to zero, injected electrons (holes) can be stored in the a-Si:H layer because of the discontinuity of the conduction (valence) band edges at the a-SiC:H/a-Si:H interfaces. By

applying a negative (positive) gate bias, holes (electrons) are injected from the substrate into the a-Si:H layer through the graded a-SiC:H layer and recombine with the stored electrons (holes) and thus the memory is erased." Sakata, columns 1 and 2.

Burns emphasizes the different principles of operation of a floating gate transistor such as disclosed by Sugita and the principles of operation of the HJ diode structure of Sakata quoted above. Burns describes the programming of a floating gate transistor with the language: "[e]lectrons are accelerated, ...and acquire enough energy to enter the conduction band of the gate oxide layer. There they are attracted by the positive potential on the select gate, and many of them lodge on the floating gate." Burns, page 383. Burns then describes the erasure of the floating gate transistor with UV light: "[t]he UV light imparts photon energy to the electrons, allowing them to escape through the oxide layer." Burns, page 383. Unlike the operation of the HJ diode structure of Sakata, only electrons are involved in programming and erasing a floating gate transistor.

The principles of operation of the floating gate transistor of Sugita are therefore substantially different from the principles of operation of the HJ diode structure of Sakata. An addition of elements from Sugita to the HJ diode structure of Sakata would change the principle of operation of Sakata, and therefore the teachings of Sakata and Sugita are not sufficient to render claim 24 *prima facie* obvious.

Two statements in Sakata refer to memory devices. Sakata states that "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." Sakata, column 1. Later, Sakata states that "the present structure can be used as a component of dynamic random access memories (DRAMS)." Sakata, column 3. Sakata is **not** here stating that the HJ structure is a floating gate transistor, but may be merely expressing the hope that the HJ diode structure can be used in some unspecified type of memory device. The C-V plot of Sakata shows a "large hysteresis" that may be used as a memory window. Sakata, column 2. While the hysteresis shown in the C-V plot may be used to create a device to store data, this is **not** a suggestion that the HJ diode structure of Sakata can be combined with elements of the floating gate transistor of Sugita.

The Office Action states that the motivation for combining Sakata and Sugita is that "the source, drain, and channel regions allow individual floating gate devices to be formed in an array....[t]he use of the source/drain/channel regions for such programming is well known in the art." Office Action, text bridging pages 5-6. Examiner Eckert and the applicant's representative Mr. Mates discussed a recent Federal Circuit opinion, *In re Sang Su Lee*, 00-1158 (Fed. Cir. January 18, 2002), which specifically required that the suggestion or motivation to combine references "must be based on objective evidence of record." The court also state that "[t]his factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority." The office action did not cite evidence in the record, such as one of the references, that supports the above-stated motivation for combining Sakata and Sugita. The applicant respectfully submits that there is no suggestion in the record for the combination of Sakata and Sugita.

The applicant respectfully submits that a *prima facie* case of obviousness of claim 24 has **not** been established in the Office Action, and that claim 24 is in condition for allowance. Claims 25-28 and 44 are dependent on claim 24, and recite further limitations with respect to claim 24. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 25-28 and 44 has **not** been established in the Office Action, and that claims 25-28 and 44 are in condition for allowance.

Claims 2, 3, 41-43, 45-48, 50-52, and 65-68 recite elements similar to those recited in claim 24. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 2, 3, 41-43, 45-48, 50-52, and 65-68 has **not** been established in the Office Action, and that claims 2, 3, 41-43, 45-48, 50-52, and 65-68 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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Date 21 March 2002 By _____

Robert E. Mates
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CERTIFICATE UNDER 37 CFR 1:8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 21st day of March, 2002.

Name Amy Moriarty Signature _____